AMENDMENTS TO THE CLAIMS

1-8. **(Canceled)**

9. **(Currently Amended)** A task switching apparatus for switching tasks to be executed in a processor by switching time slots to which a task is assigned, comprising:

a first generating unit operable to assign, on a one-to-one basis, first time slots in a plurality of time slots within a period to each first task among a plurality of first tasks whose assignment time is specified, and generate time slot information including assignment time of each first task corresponding to each of the first time slots;

a second generating unit operable to assign a plurality of second tasks, each with a priority classification, to a single second time slot among the plurality of time slots within the period, and generate time slot information including an assignment time and at least one priority classification of at least one second task assigned to the second time slot;

a time slot switching unit operable to switch time slots when an execution time of a task reaches an assignment time;

a third generating unit operable to generate task management information including an address of each of tasks assigned to a time slot;

a storing unit operable to store the generated time slot information and task management information in association with each other;

a selecting unit operable to select time slot information stored in said storing unit at least once in the period;

a control unit operable to allow an execution of a task indicating task management information corresponding to the time slot information when time slot information to which a first task is assigned is selected, select a task from a plurality of task management information corresponding to the time slot information according to priority classifications and allow an execution of the task indicated by the selected task management information when time slot information to which at least one second task is assigned is selected;

a memory unit ~~in which~~ configured to store programs for causing said ~~respective units~~ first generating unit, said second generating unit, said time slot switching unit, said third

generating unit, said storing unit, said selecting unit, and said control unit to perform their respective functions ~~function are stored~~; and

a processor which executes the programs.

10. **(Previously Presented)** The task switching apparatus according to Claim 9,

wherein said storing unit stores task management information of the plurality of second tasks as a queue in which the task management information is aligned in order of priority classifications , and

said control unit selects tasks corresponding to leading task management information of the queue.

11. **(Previously Presented)** The task switching apparatus according to Claim 10,

wherein said second generating unit sets a difference between the period and total assignment times of all first tasks in the corresponding time slot information as an assignment time of the second time slot.

12. **(Previously Presented)** The task switching apparatus according to Claim 11,

wherein said second generating unit recalculates the residual time so as to determine an assignment time of the second time slot every time said first generating unit assigns a time slot to a new first time slot.

13. **(Previously Presented)** The task switching apparatus according to Claim 12 wherein said storing unit further stores lock information regarding whether a resource capable of being accessed by a task is in a lock state , the task switching apparatus further comprising:

a queue managing unit operable to dissociate task management information of the task stored in said storing unit from time slot information when a task under execution attempts to access a resource in a lock state, have said storing unit store the task management information as a wait queue, and have said storing unit store task management information in a wait queue in association with time slot information when the resource is unlocked.

14. **(Previously Presented)** The task switching apparatus according to Claim 13 wherein the processor includes at least two register sets for storing contexts of tasks, further comprising:

a register set switching unit operable to prepare one of the register sets used for a task under execution, return the context of a task to be executed next to another register set using background processing and switch register sets when switching time slots.

15-17. **(Canceled)**